Attorney Docket No. 0756-0864

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2871
Yasuhiko TAKEMURA	)	Examiner: Tai V. Duong
Serial No. 08/051,313	)	CERTIFICATE OF MAILING
Filed: April 23, 1993	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 30, 2008.
For: ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME	)	Adelin Stamper

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), Appellants submit this *Appeal Brief* to appeal the examiner's final rejection of claims 121-123, 125, 126, 128, 142-145, 147-150, 152 and 159-165 in the Official Action mailed October 31, 2007, and maintained in the *Advisory Action* mailed March 28, 2008. A *Notice of Appeal* was filed April 30, 2008.

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I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellants, their legal representatives, and the assignee are not aware of any other prior or pending appeals, interferences or judicial proceedings which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1, 3, 5, 50, 53-55, 58, 61, 62, 65-67, 70, 74, 75, 78, 81, 85, 86, 92, 95, 98-100, 103, 106, 107, 110-112, 115, 118 and 121-165 are pending in the present application, of which claims 1, 5, 50, 53-55, 58, 61, 62, 65-67, 70, 74, 75, 78, 81, 121, 125, 129, 133, 137, 139, 142, 148 and 153 are independent. The Applicant notes with appreciation the allowance of claims 1, 3, 5, 50, 53-55, 58, 61, 62, 65-67, 70, 74, 75, 78, 81, 85, 86, 92, 95, 98-100, 103, 106, 107, 110-112, 115, 118, 129-141 and 153-158 and the indication of the allowability of claims 124, 127, 146 and 151 (pages 4-6, Paper No. 20071028). (The Examiner appears to have inadvertently omitted claim 5 from the list of allowed claims at Box 5 of the Office Action Summary of the Final Official Action and at Box 7 of the *Advisory Action*. However, the record is clear that claim 5 is allowed, for example, at pages 5-6 of the Final Official Action.) Claims 121-123, 125, 126, 128, 142-145, 147-150, 152 and 159-165 stand rejected, of which claims 121, 125, 142 and 148 are independent.

IV. STATUS OF AMENDMENTS

All prior amendments are believed to have been entered in the present application. Thus, the status of the claims in this application is as set forth above and in Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Each of independent claims 121, 125, 142 and 148 recites an electro-optical device of an active matrix comprising: a gate line of n-th row provided over a substrate; a gate line of (n+1)-th row provided over said substrate; a data line of m-th column provided over said substrate; a first pixel electrode provided over said substrate and electrically connected with said data line and said gate line of n-th row through at least one transistor; and a second pixel electrode provided over said substrate and electrically connected with said data line and said gate line of (n+1)-th row through at least one transistor, wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode, which is supported in the present specification, for example, by at least Figure 1(B) of the subject application, reproduced below.

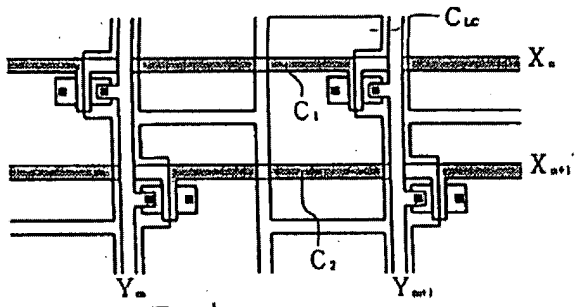


Fig. 1(B)

Also, claims 121, 125, 142 and 148 recite wherein a bipolar pulse is applied to the gate line of n-th row, and wherein the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse, which is supported in the present specification, for example, by at least by page 11 of the specification and Figure 3(B) of the subject application, reproduced below.

> applying a bipolar pulse comprising two pulses having opposite polarities to each other to said first gate line. The pixel electrode is superposed on the first gate line with an insulator therebetween.

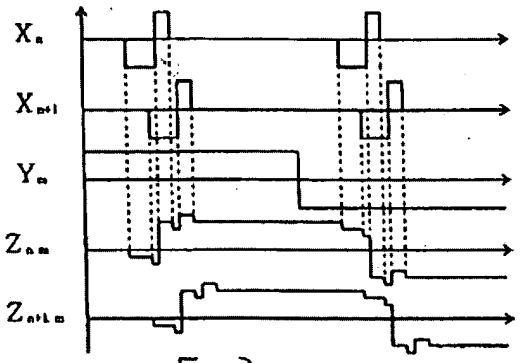


Fig.3(B)

Further, claims 121 and 142 recite wherein a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse, which is supported in the present specification, for example, by at least pages 11-12 of the specification, and Figures 1(D) and 3(B), shown below.

The operations of these circuits are shown in Figs. 3(A) and 3(B). Fig. 3(A) shows a driving operation for the circuit as shown in Figs. 1(A) and 1(C), and Fig. 3(B) shows a driving operation for the circuit as shown in Figs. 1(B) and 1(D). In a case where there is a time lag between a pulse which is applied for the purpose of driving the picture element (TFT) concerned and a pulse which is applied for the purpose of canceling

(offsetting) ΔV, the voltage is temporally varied, but returned to its original state. Therefore, affection of such variation of the voltage on an image is very slight, and thus it is visually unidentifiable.

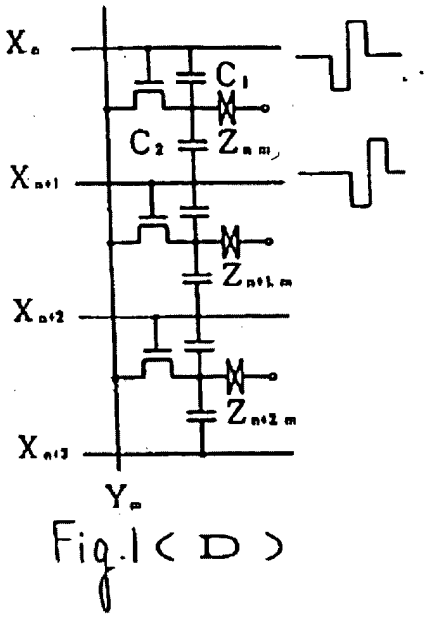


Fig.1(D)

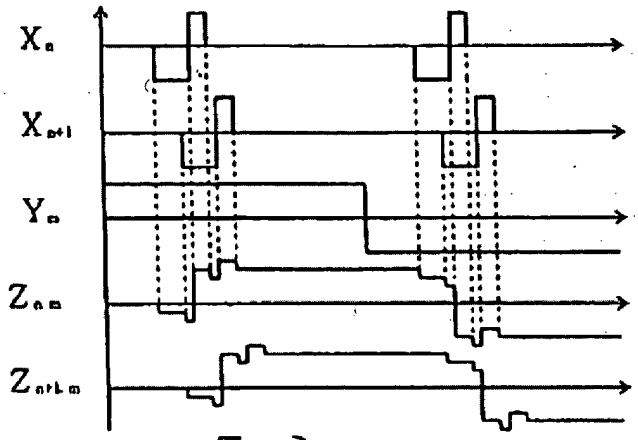


Fig.3(B)

Still further, claims 142 and 148 recite wherein a pulse width of the first pulse is different from a pulse width of the second pulse, which is supported in the present specification, for example, by at least Figure 3(B), reproduced above.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 121-123, 125, 126, 128, 142, 143-145, 147-150, 152 and 159-165 are anticipated by U.S. Patent No. 4,775,861 to Saito. The rejected independent claims 121, 125, 142 and 148 shall not stand or fall together. Independent claims 142 and 148 (and dependent claims) further recite that a pulse width of the first pulse is different from a pulse width of the second pulse and are separately patentable for at least this reason.

B. Whether dependent claims 159-165 fail to comply with the written description requirement under 35 U.S.C. § 112, first paragraph.

C. Whether the recited feature "a driving circuit ... for generating bipolar pulse(s)" of dependent claims 159-165 must be shown in the drawings or the features canceled from the claims under 37 CFR § 1.83(a) and whether the specification fails to provide proper antecedent basis for the claimed subject matter.

VII. ARGUMENTS

A. Whether claims 121-123, 125, 126, 128, 142, 143-145, 147-150, 152 and 159-165 are anticipated by U.S. Patent No. 4,775,861 to Saito.

The Official Action rejects claims 121-123, 125, 126, 128, 142, 143-145, 147-150, 152 and 159-165 as anticipated by U.S. Patent No. 4,775,861 to Saito. The Applicant respectfully traverses the rejection because the Official Action has not established an anticipation rejection.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicant respectfully submits that an anticipation rejection cannot be maintained against independent claims 121, 125, 142 and 148 of the present application. Claims 121, 125, 142 and 148 positively recite "a first bipolar pulse" and "a second bipolar pulse" or "a bipolar pulse." These features are not mere statements of the intended use of the electro-optical device. Rather, the Applicant has claimed an electro-optical device in operation, where the device in operation includes a bipolar pulse or first and second bipolar pulses applied to a gate line. Specifically, claims 121 and 142 recite that a first bipolar pulse is applied to a gate line of n-th row during a first period, a second bipolar pulse is applied to a gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and that each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse. Claims 125 and 148 recite that a

bipolar pulse is applied to a gate line of n-th row, and that the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse. For the reasons provided below, the Applicant respectfully submits that Saito does not teach the above-referenced features of the present invention, either explicitly or inherently.

The Official Action appears to concede that Saito does not teach or suggest the above-referenced features of the independent claims. The Official Action has not presented a *prima facie* case of anticipation demonstrating that a single prior art reference teaches all the features of the present invention, either explicitly or inherently. Rather, the Official Action has attempted to ignore the above-referenced features by asserting that the features are mere intended use and by citing the Board's decision in Ex parte Masham. Specifically, the Official Action asserts the following at page 4, lines 3-11 (emphasis added):

> The recited feature "wherein a first bipolar pulse is applied to the gate line ... to the first pulse" has not been given patentable weight because it is directed to the manner of operating the device. It has been recognized that the manner of operating the device does not differentiate apparatus claim from the prior art. A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP 2114, page 2100-56.

The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The independent claims of the present application clearly and positively recite an electro-optical device comprising, for example, a first bipolar pulse applied to a gate line of n-th row and a second bipolar pulse applied to a gate line of (n+1)-th row, or a bipolar pulse applied to a gate line. The bipolar pulses are components of the claimed electro-optical device in operation and not mere statements of intended use. The Applicant has claimed a device in operation including the bipolar pulses. There is no prohibition against an Applicant claiming a device in operation. Also, in a claim directed to a device in operation, positively recited features are not statements of mere intended use of the device. A claim directed to a device in operation may be differentiated from a

device claim where the intended use of the device is set forth in the preamble in a phrase beginning with "for" or where a given structural feature "is adapted" for an intended function or "is capable" of having an intended function. Such types of "intended use" language are not used in the present claims. For example, the Applicant is not merely claiming a gate line that may be adapted to receive a bipolar pulse. Rather, the Applicant is clearly and positively reciting that the present electro-optical device includes a bipolar pulse and a gate line, and the bipolar pulse is applied to the gate line.

When one of ordinary skill in the art at the time of the present invention operates the device of Saito, one would not have known to generate bipolar pulses and apply those pulses to the gate lines. There is no intention in Saito to apply a bipolar pulse to a gate line. If there was an intent to apply a bipolar pulse to the gate line in Saito, there would have been a disclosure of such fact. Absent this disclosure, anticipation has not been proven.

Also, the present claims are clearly differentiated from the claims in question in Ex parte Masham. MPEP § 2114 states the following (emphasis added):

> A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing ..., said mixing means being stationary and completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.).

In Ex parte Masham, the Board maintained the positively recited features of the claims, i.e. a mixer and flowing developer material. However, the Board did not give patentable weight to the statement "for mixing flowing developer material" or that the mixer is "completely submerged in the developer material." In Ex parte Masham, the device of the prior art could be operated completely submerged and it was just as likely

to be operated submerged as not. Also, the prior art differed from the claim in question as a matter of degree. Specifically, the prior art in Ex parte Masham, disclosed partial submersion of a mixer. However, in the present application, Saito cannot be operated to create a bipolar pulse and it would not have been just as likely for one of ordinary skill in the art at the time of the present invention to operate Saito in a manner such that a bipolar pulse is generated and applied to the gate lines, much less that such pulses could or should be applied in the manner as presently claimed. Also, Saito does not differ from the present claims by a mere matter of degree. Rather, Saito fails to teach a bipolar pulse, either explicitly or inherently.

Therefore, the Official Action has not demonstrated that Saito teaches all the limitations of the present claims. Saito is completely silent as to the use of a bipolar pulse. Specifically, Saito does not teach (1) that a first bipolar pulse is applied to a gate line of n-th row during a first period, a second bipolar pulse is applied to a gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and that each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse; or (2) that a bipolar pulse is applied to a gate line of n-th row, and that the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse, either explicitly or inherently.

The *Advisory Action* mailed March 28, 2008, newly asserts that "the recited feature 'wherein a bipolar pulse is applied to the gate line ... to the first pulse' is equivalent to a step of applying a bipolar pulse to the gate line of a driving method or operating method of a LCD, as recognized in the art and as evidence by the instant original driving method claims 9-20 filed on 04/23/1993" (page 2, Paper No. 20080324). The Applicant respectfully disagrees and traverses the above-referenced assertions in the *Advisory Action*. Initially, it is noted that claims 9-20 of the original driving method filed on April 23, 1993, have absolutely no relevance to the question of whether Saito anticipates the features of the present independent claims 121, 125, 142 and 148. For the reasons noted above, Saito does not teach the features of the present invention, either explicitly or inherently.

Independent claims 142 and 148 further recite that a pulse width of the first pulse is different from a pulse width of the second pulse and are believed to be separately patentable for at least this reason. As Saito is completely silent as to the use of a bipolar pulse, Saito is also necessarily completely silent as to any difference in the pulse width of a first and second pulse. Such features are not inherent in Saito and claim 142 and 148 are believed to be further patentable based on these recitations.

Since Saito does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

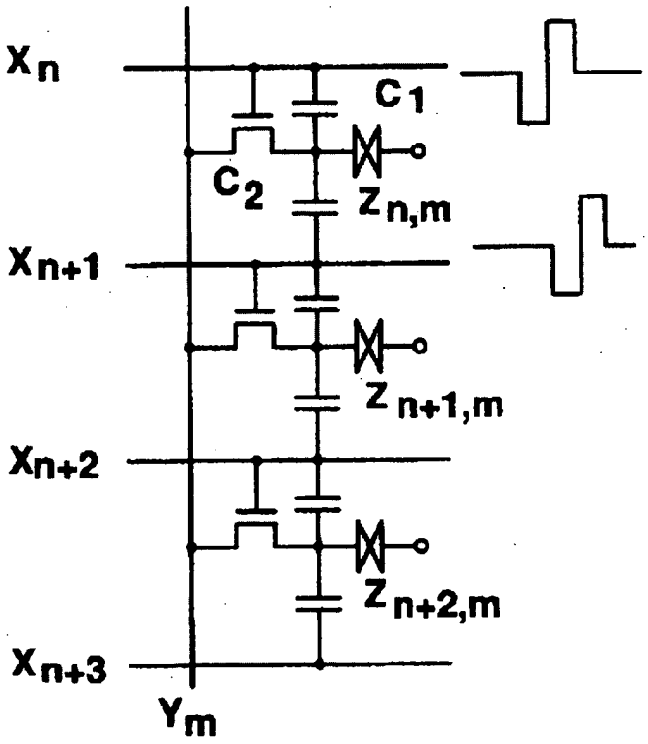
B. Whether dependent claims 159-165 fail to comply with the written description requirement under 35 U.S.C. § 112, first paragraph.

The Official Action rejects claims 159-165 under 35 U.S.C. § 112, first paragraph, "as failing to comply with the written description requirement" (page 3, Paper No. 20071028). Specifically, the Official Action asserts that "[n]owhere in the original specification does it disclose 'a driving circuit connected to the gate lines for generating a bipolar pulse or first and second bipolar pulses' ..." (Id.). The Official Action is implying that a lack of explicit disclosure for a given term is insufficient to comply with the written description requirement of § 112, first paragraph. While the Applicant concedes that the specification does not explicitly disclose a "driver circuit," the Applicant respectfully submits that explicit disclosure is not required to comply with the written description requirement, and, for at least this reason, the Applicant disagrees and traverses the assertions in the Official Action.

As noted in MPEP § 2163, "[w]hile there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure" (emphasis added). Also, "[t]he fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now

claimed. See, e.g., Vas-Cath, Inc., 935 F.2d at 1563-64, 19 USPQ2d at 1117." The Applicant respectfully submits that the features of claims 159-165 are supported in the present specification through express, implicit and inherent disclosure. Also, the Applicant respectfully submits that the present specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, the Applicant was in possession of the invention as now claimed.

The Official Action appears to question the written description of "a driving circuit connected to the gate lines for generating a bipolar pulse or first and second bipolar pulses." It is important to note that the present specification literally and explicitly supports gate lines, a bipolar pulse and first and second bipolar pulses. For example, Figure 1(D) of the present specification (reproduced below) appears to show examples of gate lines and first and second bipolar pulses.



The features of Figure 1(D) are described in the present specification, for example as follows: "gate line (X_n) is in parallel with the gate line (X_{n+1}) ... capacitances C_1 and C_2 ... the gate line is required to be supplied with a bipolar pulse comprising a

combination of a positive pulse and a negative pulse ... In a picture element $Z_{n,m}$, C_2 is supplied with a pulse for driving a picture element $Z_{n+1,m}$" (pages 10-11).

In the *Supplemental Amendment* filed July 3, 2007, the Applicant sets forth a detailed discussion as to how the present specification supports the features of independent claims 121, 125, 129, 133, 142, 148 and 153, including the following: "that a bipolar pulse is applied to the gate line of n-th row and that the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse," and "that a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period" (see pages 32-34). The Official Action does not appear to dispute the support for the above-referenced features of claims 121, 125, 129, 133, 142, 148 and 153. Therefore, the only issue that appears to be raised by the present rejection under § 112, first paragraph, is whether the present specification provides a written description for the first portion of dependent claims 159-165, *i.e.* "a driving circuit" for generating the admittedly fully supported bipolar pulse or pulses.

The Applicant respectfully submits that a driving circuit connected to the gate lines for generating a bipolar pulse or first and second bipolar pulses is disclosed in the present specification through express, implicit and inherent disclosure. Also, the Applicant respectfully submits that the present specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, the Applicant was in possession of the driving circuit as now claimed.

As noted in the *Supplemental Amendment* filed July 3, 2007, the features of claims 159-165 are disclosed in the subject application, for example, in the paragraph bridging pages 11-12, which discusses a driving operation in accordance with the present invention. Although the details of the driving circuitry are not specifically disclosed, such circuitry to generate the waveforms disclosed and claimed in the subject application was well within the level of ordinary skill in the art at the time the application was filed. It is well established that "not everything necessary to practice the invention need be disclosed. In fact, what is well-known is best omitted. In re

Buchner, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991). All that is necessary is that one skilled in the art be able to practice the claimed invention, given the level of knowledge and skill in the art." MPEP § 2164.08.

Also, the title of the present application is "ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME" (emphasis added). The driving of a picture element is discussed in detail, for example, at page 8, line 28, to page 12, line 4. Specifically, for example, the specification discloses the following at page 10, line 24, to page 11, line 21 (emphasis added):

> An equivalent circuit of FIG. 1(B) is shown in FIG. 1(D). In this case, as shown in FIG. 1(D), the gate line is required to be supplied with a bipolar pulse comprising a combination of a positive pulse and a negative pulse. This is because when one gate line is selected, another gate line is required to be supplied with a voltage having opposite polarity. In a picture element $Z_{n,m}$, C_2 is supplied with a pulse for driving a picture element $Z_{n+1,m}$, and thus the voltage of the picture element is temporally affected.

As such, the specification clearly discloses a gate line, a bipolar pulse supplied to the gate line, and the timing of the bipolar pulse (see, e.g., Figure 1(D), reproduced above). Therefore, the Applicant was clearly in possession of a circuit to make these pulses at the time the invention was made. The Applicant respectfully submits that one of ordinary skill in the art, upon consulting the present specification, would readily understand that the bipolar pulse described in the present application is generated by a driving circuit, and that the driving circuit would be provided to generate the bipolar pulse that is supplied to the gate line. This is particularly true given the fact that the present specification explicitly discloses "driving a picture element," "driving an electro-optical device," that "FIG. 3(A) shows a driving operation for the circuit as shown in FIGS. 1(A) and 1(C), and FIG. 3(B) shows a driving operation for the circuit as shown in FIGS. 1(B) and 1(D)," "driving the picture element (TFT)," and "driving methods for the active matrix circuits of the prior art and this invention."

The *Advisory Action* mailed March 28, 2008, newly asserts that the "Applicant did not specifically point out which portions of the original disclosure disclose 'a driving circuit connected to the gate lines for generating a bipolar pulse or first and second bipolar pulses,'" that "the examiner did not agree with Applicant's remarks that the

above driving circuit is inherent in the instant specification unless Applicant provides evidences that there is only one driving circuit known in the art being capable for generating bipolar pulses," and that "it is unclear how can a driving circuit be inherent to bipolar pulses" (page 2, Paper No. 20080324). The Applicant respectfully disagrees and traverses the above-referenced assertions in the *Advisory Action*.

The Applicant has, in fact, provided specific references to the original disclosure to explain that a driving circuit connected to the gate lines for generating a bipolar pulse or first and second bipolar pulses is disclosed in the present specification through express, implicit and inherent disclosure. Although the Applicant has not limited their demonstration of support to express disclosure, some examples of "specific references" to the original disclosure include the title of the present application; the driving of a picture element described at page 8, line 28, to page 12, line 4 (specifically page 10, line 24, to page 11, line 21); Figures 1(A)-1(D), 3(A) and 3(B). Also, the Applicant has not relied solely on express disclosure, but has also set forth a detailed argument (above) as to how the present specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, the Applicant was in possession of the driving circuit as presently claimed.

The Applicant did not, in fact, argue that "the above driving circuit is inherent in the instant specification." Rather, the Applicant argued, as noted in detail above, that the features of dependent claims 159-165 are supported in the present specification through a combination of express, implicit and inherent disclosure. Also, it is not at all clear how the Examiner's requirement for evidence "that there is only one driving circuit known in the art being capable for generating bipolar pulses" is relevant to the question of whether the present specification provides a demonstration that the Applicant had possession, under § 112, first paragraph, of an invention including a driver circuit as presently claimed.

Therefore, the Applicant respectfully submits that claims 159-165, when read in light of the specification, are adequately described and supported in the specification. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

C. Whether the recited feature "a driving circuit ... for generating bipolar pulse(s)" of dependent claims 159-165 must be shown in the drawings or the features canceled from the claims under 37 CFR § 1.83(a) and whether the specification fails to provide proper antecedent basis for the claimed subject matter.

The Official Action objects to the drawings under 37 CFR § 1.83(a) asserting that "the recited feature 'a driving circuit ... for generating bipolar pulse(s)' of claims 159-165 must be shown or the feature(s) canceled from the claim(s)" (page 2, Paper No. 20071028). However, as noted above, Figure 1(D) provides an example of gate lines and first and second bipolar pulses. Although a driving circuit is not explicitly shown, as noted above, one of ordinary skill in the art upon reviewing the present specification would understand that a driving circuit is provided to generate the bipolar pulses and is connected to the gate lines. As noted in 35 U.S.C. § 113, "The applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented." In the present application, the Applicant respectfully submits that it is not believed to be strictly necessary to provide a drawing illustrating a driving circuit in order for one of ordinary skill in the art to understand the subject matter to be patented, particularly in light of the clear illustration of gate lines and first and second bipolar pulses.

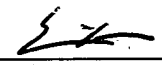
The *Advisory Action* mailed March 28, 2008, newly asserts that the "nowhere in 37 CFR 1.83(a) states that if the drawings are not necessary for the understanding of the subject matter to be patented, the drawings do not must [sic] show every feature of the invention specified in the claims" (page 2, Paper No. 20080324). However, the Applicant did not characterize Rule 83(a) in this manner. Rather, the Applicant argued that "one of ordinary skill in the art upon reviewing the present specification would understand that a driving circuit is provided to generate the bipolar pulses and is connected to the gate lines" and noted that 35 U.S.C. § 113 merely requires that "[t]he applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented."

Accordingly, reconsideration and withdrawal of the objections are in order and respectfully requested.

The Official Action objects to the specification "as failing to provide proper antecedent basis for the claimed subject matter" (page 2, Paper No. 20071028). Specifically, the Official Action asserts that "the specification does not disclose the feature 'a driving circuit connected to said gate line ... for generating bipolar pulse(s)" (pages 2-3, Id.). For the reasons noted above, the Applicant respectfully submits that the specification provides proper antecedent basis for a driving circuit for generating bipolar pulses.

For all of the above reasons, the present application is believed to be in condition for allowance and favorable reconsideration is respectfully requested. If the Examiner feels further discussions would expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Respectfully submitted,



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VIII. APPENDICES

APPENDIX A

PENDING CLAIMS

1. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween.

2. (Canceled)

3. (Previously Presented) An electro-optical device according to claim 1 wherein said capacitive wiring is in parallel with said gate line.

4. (Canceled)

5. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a gate line of (n+2)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a pixel electrode of n-th row and m-th column provided over said substrate and connected with said data line and said gate line of n-th row through corresponding at least one transistor; said pixel electrode overlapping said gate line of (n+1)-th row with an insulator therebetween and overlapping said gate line of n-th row with an insulator therebetween; and

a pixel electrode of (n+1)-th row and m-th column provided over said substrate and connected with said data line and said gate line of (n+1)-th row through corresponding at least one transistor, said pixel electrode of (n+1)-th row and m-th column overlapping said gate line of (n+2)-th row with an insulator therebetween and overlapping said gate line of (n+1)-th row with an insulator therebetween,

wherein said pixel electrode of n-th row and m-th column is provided on an opposite side of said data line to said pixel electrode of (n+1)-th row and m-th column.

6.-49. (Canceled)

50. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the

capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring.

51.-52. (Canceled)

53. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel

electrode with said insulating flattening film interposed therebetween,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring.

54. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

55. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance

between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring, and

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to the capacitive wiring.

56.-57. (Canceled)

58. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a reverse stagger type amorphous silicon thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region over said gate electrode with a gate insulating film interposed therebetween, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said reverse stagger type amorphous silicon thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel

electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

59.-60. (Canceled)

61. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive

wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween.

62. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel

electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring.

63.-64. (Canceled)

65. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring.

66. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

67. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between

the transparent pixel electrode and the capacitive wiring, and

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to the capacitive wiring.

68.-69. (Canceled)

70. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating flattening film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein a sum of a capacitance between the transparent pixel electrode and the

gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

71.-73. (Canceled)

74. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a pixel electrode provided over said insulating film wherein said pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said pixel electrode with said insulating film interposed therebetween,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

75. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line provided over a substrate;

a data line provided over said substrate;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said gate line, a channel region, a source region and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

a capacitive wiring provided over said substrate;

an insulating film over said gate line, said data line, said capacitive wiring and said thin film transistor;

a pixel electrode provided over said insulating film wherein said pixel electrode overlaps said gate line and said capacitive wiring and is electrically connected to the

other of said source region and said drain region; and

a capacitance formed between said capacitive wiring and said pixel electrode with said insulating film interposed therebetween,

wherein a sum of a capacitance between the pixel electrode and the gate line and the capacitance between the pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the pixel electrode and the gate line and the capacitance between the pixel electrode and the capacitive wiring,

wherein when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to said capacitive wiring, and

after the application of the first pulse is stopped, the application of the second pulse is stopped.

76.-77. (Canceled)

78. (Previously Presented) An electro-optical device of an active matrix comprising:

a first gate line and a second gate line extending in parallel provided over a substrate;

a data line provided over said substrate and extending across said first and second gate lines;

a thin film transistor provided over said substrate and comprising a gate electrode electrically connected to said first gate line, a channel region, a source region

and a drain region wherein one of said source region and said drain region is electrically connected to said data line;

an insulating flattening film over said first and second gate lines, said data line, and said thin film transistor;

a transparent pixel electrode provided over said insulating flattening film wherein said transparent pixel electrode overlaps said first and second gate lines and is electrically connected to the other of said source region and said drain region; and

a first capacitance formed between said first gate line and said transparent pixel electrode with said insulating flattening film interposed therebetween; and

a second capacitance formed between said second gate line and said transparent pixel electrode with said insulating flattening film interposed therebetween,

wherein a sum of the first and second capacitances is above ten times as large as a difference between the first and second capacitances.

79.-80. (Canceled)

81. (Previously Presented) An active-matrix device comprising:

a substrate having an insulating surface;

first and second pixel electrodes arranged in a first column over said substrate;

a third pixel electrode arranged in a second column over said substrate, each of said first, second and third pixel electrodes being provided with at least one thin film transistor;

first, second and third gate lines extending in parallel over said substrate,

wherein said first gate line drives the thin film transistor associated with said first pixel electrode and said first pixel electrode overlaps said first gate line to form a first capacitance therebetween;

said second gate line drives the thin film transistor associated with the third pixel electrode and extends below said first pixel electrode to form a second capacitance between said second gate line and said first pixel electrode;

said third gate line drives the thin film transistor associated with the second pixel electrode and extends below said third pixel electrode to form a third capacitance between said third gate line and said third pixel electrode,

wherein a sum of the first and second capacitances is above ten times as large as a difference between the first and second capacitances.

82.-84. (Canceled)

85. (Previously Presented) The electro-optical device of claim 74, wherein the pixel electrode is transparent.

86. (Previously Presented) The electro-optical device of claim 75, wherein the pixel electrode is transparent.

87.-91. (Canceled)

92. (Previously Presented) The electro-optical device of claim 78, wherein the thin film transistor is a reverse stagger type amorphous silicon thin film transistor.

93.-94. (Canceled)

95. (Previously Presented) The electro-optical device of claim 50, wherein the insulating flattening film comprises polyimide.

96.-97. (Canceled)

98. (Previously Presented) The electro-optical device of claim 53, wherein the insulating flattening film comprises polyimide.

99. (Previously Presented) The electro-optical device of claim 54, wherein the insulating flattening film comprises polyimide.

100. (Previously Presented) The electro-optical device of claim 55, wherein the insulating flattening film comprises polyimide.

101.-102. (Canceled)

103. (Previously Presented) The electro-optical device of claim 58, wherein the insulating flattening film comprises polyimide.

104.-105. (Canceled)

106. (Previously Presented) The electro-optical device of claim 61, wherein the insulating flattening film comprises polyimide.

107. (Previously Presented) The electro-optical device of claim 62, wherein the insulating flattening film comprises polyimide.

108.-109. (Canceled)

110. (Previously Presented) The electro-optical device of claim 65, wherein the insulating flattening film comprises polyimide.

111. (Previously Presented) The electro-optical device of claim 66, wherein the insulating flattening film comprises polyimide.

112. (Previously Presented) The electro-optical device of claim 67, wherein the insulating flattening film comprises polyimide.

113.-114. (Canceled)

115. (Previously Presented) The electro-optical device of claim 70, wherein the insulating flattening film comprises polyimide.

116.-117. (Canceled)

118. (Previously Presented) The electro-optical device of claim 78, wherein the insulating flattening film comprises polyimide.

119.-120. (Canceled)

121. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first pixel electrode provided over said substrate and electrically connected with said data line and said gate line of n-th row through at least one transistor; and

a second pixel electrode provided over said substrate and electrically connected with said data line and said gate line of (n+1)-th row through at least one transistor,

wherein said first pixel electrode is provided on an opposite side of said data line

to said second pixel electrode,

wherein a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and

wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse.

122. (Previously Presented) The electro-optical device according to claim 121 wherein the first pulse has a negative potential and the second pulse has a positive potential.

123. (Previously Presented) The electro-optical device according to claim 121 wherein the second pulse appears after the first pulse without an interruption.

124. (Previously Presented) The electro-optical device according to claim 121 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

125. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first pixel electrode provided over said substrate and electrically connected with said data line and said gate line of n-th row through at least one transistor; and

a second pixel electrode provided over said substrate and electrically connected with said data line and said gate line of (n+1)-th row through at least one transistor,

wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode,

wherein a bipolar pulse is applied to the gate line of n-th row, and

wherein the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse.

126. (Previously Presented) The electro-optical device according to claim 125 wherein the first pulse has a negative potential and the second pulse has a positive potential.

127. (Previously Presented) The electro-optical device according to claim 125 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

128. (Previously Presented) The electro-optical device according to claim 125 wherein the second pulse appears after the first pulse without an interruption.

129. (Previously Presented) An electro-optical device of an active matrix

comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first reverse stagger type amorphous silicon thin film transistor having a gate electrode electrically connected to the gate line of n-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

a second reverse stagger type amorphous silicon thin film transistor having a gate electrode electrically connected to the gate line of (n+1)-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

an insulating film formed over the first and second reverse stagger type amorphous silicon thin film transistors;

a first pixel electrode provided over said insulating film and electrically connected with the other one of the source and drain regions of the first reverse stagger type amorphous silicon thin film transistor; and

a second pixel electrode provided over said insulating film and electrically connected with the other one of the source and drain regions of the second reverse stagger type amorphous silicon thin film transistor,

wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode,

wherein a first bipolar pulse is applied to the gate line of n-th row during a first

period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and

wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse.

130. (Previously Presented) The electro-optical device according to claim 129 wherein the first pulse has a negative potential and the second pulse has a positive potential.

131. (Previously Presented) The electro-optical device according to claim 129 wherein the second pulse appears after the first pulse without an interruption.

132. (Previously Presented) The electro-optical device according to claim 129 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

133. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first thin film transistor having a gate electrode electrically connected to the

gate line of n-th row, a channel region and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

a second thin film transistor having a gate electrode electrically connected to the gate line of (n+1)-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

an insulating flattening film formed over the first and second thin film transistors;

a first pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the first thin film transistor; and

a second pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the second thin film transistor,

wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode,

wherein a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period, and

wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse.

134. (Previously Presented) The electro-optical device according to claim 133 wherein the first pulse has a negative potential and the second pulse has a positive

potential.

135. (Previously Presented) The electro-optical device according to claim 133 wherein the second pulse appears after the first pulse without an interruption.

136. (Previously Presented) The electro-optical device according to claim 133 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

137. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first reverse stagger type amorphous silicon thin film transistor having a gate electrode electrically connected to the gate line of n-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

a second reverse stagger type amorphous silicon thin film transistor having a gate electrode electrically connected to the gate line of (n+1)-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

an insulating film formed over the first and second reverse stagger type

amorphous silicon thin film transistors;

a first pixel electrode provided over said insulating film and electrically connected with the other one of the source and drain regions of the first reverse stagger type amorphous silicon thin film transistor; and

a second pixel electrode provided over said insulating film and electrically connected with the other one of the source and drain regions of the second reverse stagger type amorphous silicon thin film transistor,

wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode.

138. (Previously Presented) The electro-optical device according to claim 137 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

139. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first thin film transistor having a gate electrode electrically connected to the gate line of n-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

a second thin film transistor having a gate electrode electrically connected to the

gate line of (n+1)-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

an insulating flattening film formed over the first and second thin film transistors;

a first pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the first thin film transistor; and

a second pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the second thin film transistor,

wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode.

140. (Previously Presented) The electro-optical device according to claim 139 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

141. (Previously Presented) The electro-optical device according to claim 139 wherein each of the first and second thin film transistors is a reverse stagger amorphous silicon thin film transistor.

142. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first pixel electrode provided over said substrate and electrically connected with said data line and said gate line of n-th row through at least one transistor; and

a second pixel electrode provided over said substrate and electrically connected with said data line and said gate line of (n+1)-th row through at least one transistor,

wherein a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period,

wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse, and

wherein a pulse width of the first pulse is different from a pulse width of the second pulse.

143. (Previously Presented) The electro-optical device according to claim 142 wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode.

144. (Previously Presented) The electro-optical device according to claim 142 wherein the first pulse has a negative potential and the second pulse has a positive

potential.

145. (Previously Presented) The electro-optical device according to claim 142 wherein the second pulse appears after the first pulse without an interruption.

146. (Previously Presented) The electro-optical device according to claim 142 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

147. (Previously Presented) The electro-optical device according to claim 142 wherein the pulse width of the first pulse is longer than the pulse width of the second pulse.

148. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first pixel electrode provided over said substrate and electrically connected with said data line and said gate line of n-th row through at least one transistor; and

a second pixel electrode provided over said substrate and electrically connected with said data line and said gate line of (n+1)-th row through at least one transistor,

wherein a bipolar pulse is applied to the gate line of n-th row, and

wherein the bipolar pulse includes a first pulse and a second pulse having an opposite polarity to the first pulse, and

wherein a pulse width of the first pulse is different from a pulse width of the second pulse.

149. (Previously Presented) The electro-optical device according to claim 148 wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode.

150. (Previously Presented) The electro-optical device according to claim 148 wherein the first pulse has a negative potential and the second pulse has a positive potential.

151. (Previously Presented) The electro-optical device according to claim 148 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

152. (Previously Presented) The electro-optical device according to claim 148 wherein the second pulse appears after the first pulse without an interruption.

153. (Previously Presented) An electro-optical device of an active matrix comprising:

a gate line of n-th row provided over a substrate;

a gate line of (n+1)-th row provided over said substrate;

a data line of m-th column provided over said substrate;

a first thin film transistor having a gate electrode electrically connected to the gate line of n-th row, a channel region and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

a second thin film transistor having a gate electrode electrically connected to the gate line of (n+1)-th row and source and drain regions wherein one of the source and drain regions is electrically connected to the data line;

an insulating flattening film formed over the first and second thin film transistors;

a first pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the first thin film transistor; and

a second pixel electrode provided over said insulating flattening film and electrically connected with the other one of the source and drain regions of the second thin film transistor,

wherein a first bipolar pulse is applied to the gate line of n-th row during a first period, a second bipolar pulse is applied to the gate line of (n+1)-th row during a second period, and the second period appears later than and partly overlaps the first period,

wherein each of the first and second bipolar pulses includes a first pulse and a second pulse having an opposite polarity to the first pulse, and

wherein a pulse width of the first pulse is different from a pulse width of the

second pulse.

154. (Previously Presented) The electro-optical device according to claim 153 wherein said first pixel electrode is provided on an opposite side of said data line to said second pixel electrode.

155. (Previously Presented) The electro-optical device according to claim 153 wherein the first pulse has a negative potential and the second pulse has a positive potential.

156. (Previously Presented) The electro-optical device according to claim 153 wherein the second pulse appears after the first pulse without an interruption.

157. (Previously Presented) The electro-optical device according to claim 153 wherein the first pixel electrode overlaps the gate line of n-th row and the gate line of (n+1)-th row.

158. (Previously Presented) The electro-optical device according to claim 153 wherein each of the first and second thin film transistors is a reverse stagger amorphous silicon thin film transistor.

159. (Previously Presented) The electro-optical device according to claim 121

further comprising a driving circuit connected to said gate line of n-th row and said gate line of (n+1)-th row for generating said first bipolar pulse and said second bipolar pulse.

160. (Previously Presented) The electro-optical device according to claim 125 further comprising a driving circuit connected to said gate line of n-th row for generating the bipolar pulse.

161. (Previously Presented) The electro-optical device according to claim 129 further comprising a driving circuit connected to said gate line of n-th row and said gate line of (n+1)-th row for generating said first bipolar pulse and said second bipolar pulse.

162. (Previously Presented) The electro-optical device according to claim 133 further comprising a driving circuit connected to said gate line of n-th row and said gate line of (n+1)-th row for generating said first bipolar pulse and said second bipolar pulse.

163. (Previously Presented) The electro-optical device according to claim 142 further comprising a driving circuit connected to said gate line of n-th row and said gate line of (n+1)-th row for generating said first bipolar pulse and said second bipolar pulse.

164. (Previously Presented) The electro-optical device according to claim 148

further comprising a driving circuit connected to said gate line of n-th row for generating said bipolar pulse.

165. (Previously Presented) The electro-optical device according to claim 153 further comprising a driving circuit connected to said gate line of n-th row and said gate line of (n+1)-th row for generating said first bipolar pulse and said second bipolar pulse.

APPENDIX B
REFERENCES

Copies attached.

APPENDIX C
EVIDENCE APPENDIX

Not applicable.

APPENDIX D
RELATED PROCCEDINGS APPENDIX

Not applicable.

United States Patent [19]

Saito

[11] **Patent Number: 4,775,861**

[45] **Date of Patent: Oct. 4, 1988**

[54] **DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL WHICH EQUIVALENTLY REDUCES PICTURE DEFECTS**

[75] Inventor: **Takeshi Saito, Tokyo, Japan**

[73] Assignee: **NEC Corporation, Tokyo, Japan**

[21] Appl. No.: **667,887**

[22] Filed: **Nov. 2, 1984**

[51] **Int. Cl.**[4] **G09G 3/36**

[52] **U.S. Cl.** **340/784**; 340/719; 350/333

[58] **Field of Search** 340/784, 718, 719, 765, 340/715; 365/200, 63, 149; 350/333

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,938,140	2/1976	Garcia et al.	340/765
4,023,890	5/1977	Shirasu et al.	340/765
4,301,450	11/1981	Smoliar	340/715
4,368,523	1/1983	Kawate	340/784
4,600,274	7/1986	Morozumi	340/784

FOREIGN PATENT DOCUMENTS

0186086	12/1984	European Pat. Off. .
60-97322	5/1985	Japan .
60-186823	9/1985	Japan .

OTHER PUBLICATIONS

A. J. Snell et al, "Applications of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels", Applied Physics, No. 24 (1981), pp. 357–362.

Article "Promise and Challenge of Thin-Film Silicon Approaches to Active Matrices", Lakatos, IEEE Transactions on Electron Devices, vol. ED-30, No. 5, May 1983.

Primary Examiner—Gerald L. Brigance

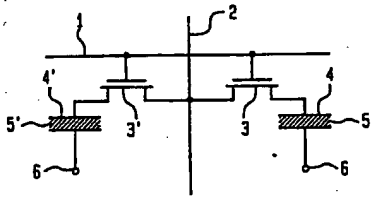
Assistant Examiner—Jeffery A. Brier

Attorney, Agent, or Firm—Burns, Doane, Swecker & Mathis

[57] **ABSTRACT**

A driving circuit of a liquid crystal display panel comprises a plurality of scanning lines, a plurality of signal lines arranged orthogonally to the scanning lines and a plurality of switching elements disposed at each of crossing points of the scanning lines and the signal lines, and liquid crystal display elements coupled to the respective switching elements, the switching elements being switched by signals at said scanning lines to drive the associated liquid crystal display elements.

10 Claims, 4 Drawing Sheets



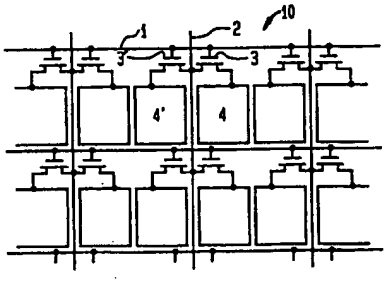


FIG. 1
(PRIOR ART)

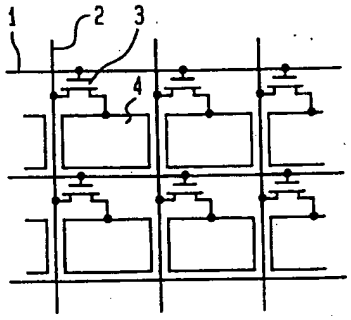


FIG. 2
(PRIOR ART)

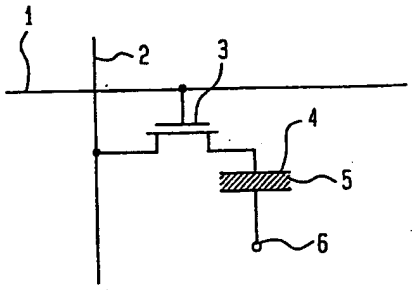


FIG. 3A

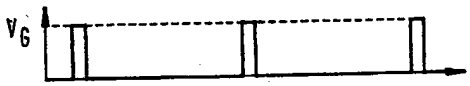


FIG. 3B

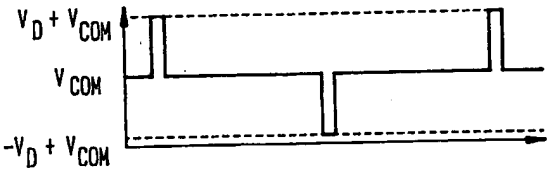


FIG. 3C

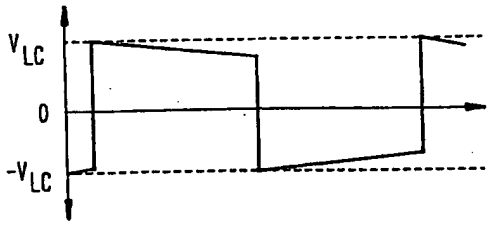


FIG. 4

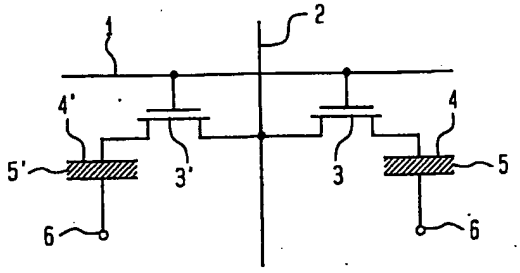


FIG. 5

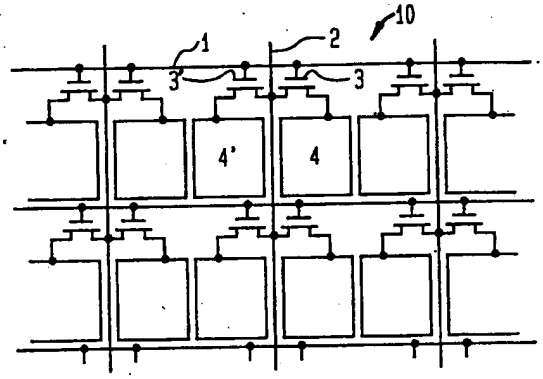


FIG. 6

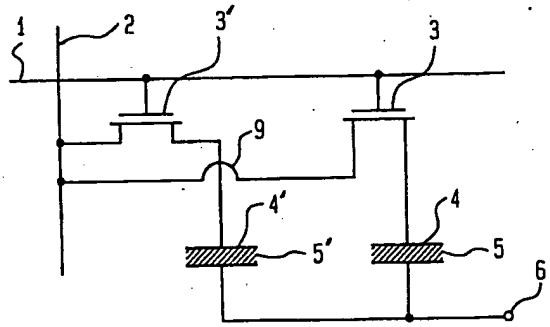


FIG.7

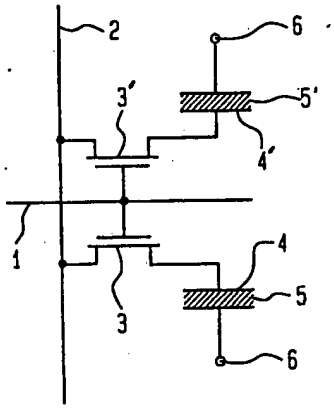


FIG.8

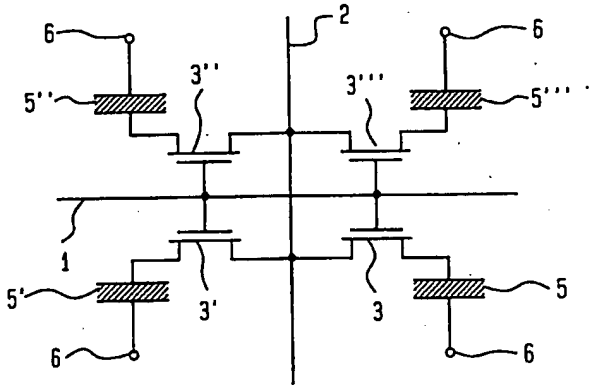
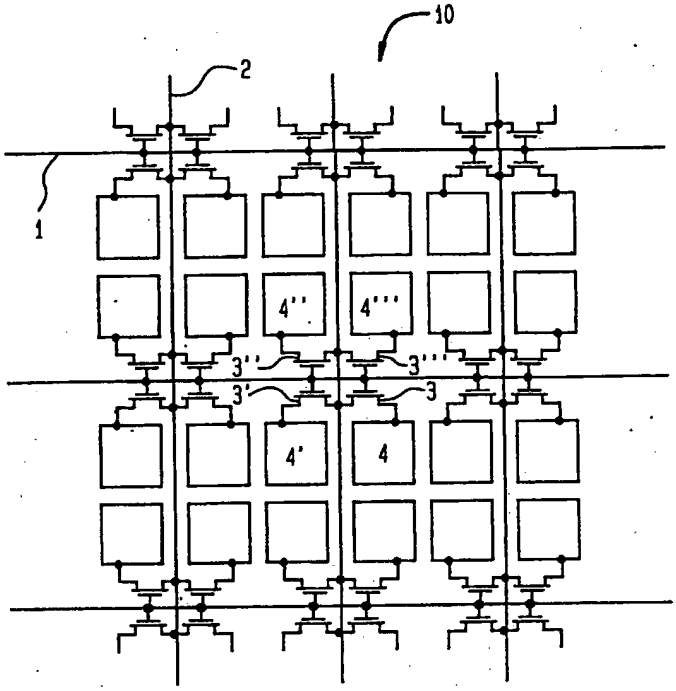


FIG. 9



DRIVING CIRCUIT OF A LIQUID CRYSTAL DISPLAY PANEL WHICH EQUIVALENTLY REDUCES PICTURE DEFECTS

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates to a driving circuit for a liquid crystal display panel, and more particularly to an improvement of the driving circuit for equivalently reducing picture defects.

2. Description of the Prior Art:

Matrix type large area displays have been developed as means for displaying graphs, characters and images. Among various kinds of such displays, liquid crystal display panels have considerable potential. A typical structure is shown in "Applied Physics" No. 24 (1981) pp. 357 to 362, A. J. Snell, et al. "Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels" and has a glass substrate on which a plurality of thin film MOS field effect transistors (hereinafter, referred to as a TFT) as switching elements are mounted in a matrix form which is covered with a transparent cover plate with liquid crystal inserted between the glass substrate and the transparent cover plate. The inner surface of the cover plate is coated with a transparent conducting layer of Indium Tin Oxide (ITO). The transmittance of the liquid crystal to respective picture elements is controlled by selectively driving the TFT's. The TFT's are formed in a polycrystalline silicon layer or an amorphous silicon layer. By use of the TFT's, the resolution rises to the extent practical, but the density of picture defects is not reduced. It is impossible by present production techniques to increase the yield of TFT's up to one. The picture elements corresponding to the defective TFT's appear as picture defects. If the yield of the TFT's is assumed as 99.9%, 250 picture defects appear on a display panel having picture elements in a matrix of 500 rows and 500 columns. Such a defective image cannot be practically used in a market. Further, the high density of picture defects limits the application of the liquid crystal display panels to small size displays.

SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide a liquid crystal display panel in which picture defects are equivalently reduced.

According to the present invention, the liquid crystal display panel comprises a plurality of scanning lines receiving scanning signals, a plurality of signal lines arranged orthogonally to the scanning lines and receiving driving signals, a plurality of sets of a plural number of switching elements, each set being disposed at a crossing point of the scanning line and the signal line and a plurality of liquid crystal elements coupled with the respective switching elements, the driving signals being applied to the liquid crystal elements through the switching elements in response to the scanning signals.

Each liquid crystal element at each crossing point of scanning and signal lines is divided into two or more in accordance with this invention, and two or more TFT's as the switching elements are disposed there to drive the divided liquid crystal elements. Therefore, if one TFT at one picture element is defective, the other TFT or TFT's drive the associated liquid crystal element or elements at that picture element. Although some of the switching elements are imperfect, it is visually seen as non-defective. Thus, the picture defects are equivalently reduced. This equivalent defect reduction is similarly obtained, even if the overall number of picture elements is made large, resulting in a possibility of application of liquid crystal to large area display panels.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is an exemplary circuit diagram of a part of driving circuit panel used in a liquid crystal display panel of the prior art;

FIG. 2 is a circuit diagram of one element of the liquid crystal display panel using the prior art driving circuit of FIG. 1;

FIG. 3 is a timing chart of a scanning signal V_G applied to scanning lines; FIG. 3*b* is a timing chart of a driving signal applied to signal lines; and FIG. 3*c* is a timing chart of voltage V_{LC} applied to the liquid crystal of a picture element;

FIG. 4 is a circuit diagram of one element of the liquid crystal display panel using the driving circuit according to a first embodiment of the present invention;

FIG. 5 is an explanatory circuit diagram of a part of driving circuit panel used in the first embodiment of the present invention;

FIG. 6 is a circuit diagram of a modification of one element of the liquid crystal display panel used in the first embodiment of the present invention;

FIG. 7 is a circuit diagram of another modification of one element of the liquid crystal display panel used in the first embodiment of the present invention;

FIG. 8 is a circuit diagram of one element of the liquid crystal display panel used in a second embodiment of the present invention; and

FIG. 9 is circuit diagram of a part of the driving circuit panel used in the second embodiment of the present invention.

A driving circuit panel in the prior art is shown in FIG. 1. A plurality of parallel scanning lines 1 are deposited on a glass substrate. A plurality of signal lines 2 are arranged orthogonally to the scanning lines 1 on the glass substrate. Every crossing accompanies one TFT3 with a gate connected to the scanning line 1, a source connected to the signal line 2 and a drain connected to a lower electrode 4. In an actual design, parts of the scanning lines 1 at the crossing with signal line 2 are used as gate electrodes of the TFT3. After the scanning lines 1 are covered with an insulator film, polycrystalline silicon or amorphous silicon is deposited on the insulator film at the parts of the scanning lines 1 as a semiconductor material. Source electrodes continuous to the signal lines 2, and drain electrodes continuous to the lower electrode 4 are formed on the semiconductor material at both sides of the scanning lines 1. Thus, TFT's 3 are formed at every crossing of scanning and signal lines.

The lower electrodes are electrodes to apply driving voltages to liquid crystal in picture elements. Thus, a prepared driving circuit panel is covered with liquid crystal via a shading film, a passivation film and an orientation film. A transparent cap having a deposited transparent conductive layer as an upper electrode on a lower surface covers the liquid crystal. The driving

voltage is applied to the liquid crystal between the lower electrode connected to TFT3 selected by scanning and signal voltage and the upper electrode. This structure is shown in FIG. 2 in the form of a circuit diagram in which the liquid crystal is referred to as the numeral 5 and the upper electrode as the numeral 6.

The scanning of TFT's 3 and the driving of liquid crystal will now be explained with reference to FIGS. 3*a*, 3*b* and 3*c*. Scanning signal V_G is an intermittent pulse having a width of several tens of μsec, a height of 12 volts and a repetition period of 16.7 msec, as shown in FIG. 3*a*. The scanning of the display is performed by shifting the phases of pulses in accordance with the scanning lines 1. The information to be reproduced on the display panel is applied on the signal lines in synchronism with the scanning signal. The signal voltage depends on the information and is lower than 10 volts. The polarity of the signal voltage is changed alternately at every scanning period to prevent the liquid crystal from deterioration. In a case where the voltage V_{com} such as a ground potential is applied to the upper electrode 6, the timing chart of the driving signal may be expressed as FIG. 3*b*. The signal voltage is charged into the liquid crystal through TFT3 selected by the scanning signal. The voltage V_{LC} across the liquid crystal is shown in FIG. 3*c*. The peak voltage is about 8 volts as a result of a voltage loss at TFT3 etc. When the voltage V_{LC} is at the peak, the liquid crystal lowers its transmitters, if the liquid crystal is of the twisted nematic type.

A problem in the prior art liquid crystal display panels is picture defects based on defective TFT's. One TFT is used at one crossing for one picture element. Therefore, the picture element coupled with the defective TFT does not work. As mentioned in the introductory part of this specification, if the yield of the TFT is 99.9%, the number of defective picture elements is 250 in a display panel having a matrix of picture elements of 500 rows and 500 columns. Such defective display does not have any worth in a market. It is impossible by the present production technique to raise the yield more than 99.9%.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 4, each picture element at each crossing of a scanning line 1 and a signal line 2 consists of two sets of a thin film MOS field effect transistor 3(3') and a liquid crystal display element with a lower electrode 4(4'), liquid crystal 5(5') and an upper electrode 6, according to the first embodiment of the present invention. Gates of the TFT's 3 and 3' are commonly connected with the scanning line 1, and their sources are also commonly connected with the signal line 2. Thus, it can be said that one conventional picture element is divided into two at each crossing. If one of the TFT's is defective, the other drives the associated liquid crystal display element, resulting in reduction of area of defective elements on the display panel. The information of the picture element is maintained on the display panel by the non-defective part with a reduced area. The visual naturalness is kept on the display panel.

One part of the driving circuit panel is explanatory shown in FIG. 5. A plurality of scanning lines 1 are formed on a glass substrate 10. A plurality of signal lines 2 are also formed on the glass substrate but isolated from the scanning lines. At every crossing of the scanning lines 1 and the signal lines 2, TFT's 3 and 3' are formed on both sides of the signal lines 2. Gates are connected wit the scanning line 1 and sources are with the signal line 2. Drains are respectively connected with lower electrodes 4 and 4' each having a width of 100 μm and a length of 200 μm. The TFT's 3 and 3' have polycrystalline silicon or amorphous silicon as a semiconductor material which is disposed on the scanning line 4 via an insulator film. The whole panel is covered with a shading film, a passivation film and an orientation film on which liquid crystal, such as the twisted nematic type is disposed. A cover plate of the liquid crystal is composed of a transparent insulator plate having a transparent conductive layer on the inner surface. The transparent condctive layer operates as a common upper electrode of the liquid crystal display elements.

Here, the yield of the TFT's is assumed as 99.9%. If the display panel has a matrix of picture elements of 500 rows and 500 columns, 500,000 liquid crystal display elements are formed and the same number of TFT's are constructed on one panel. The number of defective TFT's are 500, causing 500 non-working liquid crystal display elements. However, the number of the picture elemehts, or crossing points, where both of the two TFT's are defective is only $\frac{1}{4}$. In other words, the number of the defective picture elements is reduced to 1/500 of the prior art structure. Almost all picture elements present visual information. By determining the driving voltage such that the non-defective liquid crystal display element in a picture element including a defective TFT is driven to make the transmittance of liquid crystal double, the picture on the display panel visually becomes a non-defective picture. The transmittance of liquid crystal may be made double by raising the driving voltage in synchronism with the drive of the TFT pair including a defective TFT. One example of the synchronization is the use of semiconductor memories.

According to one modification of the first embodiment shown in FIG. 6, both of two TFT's 3 and 3' are disposed on one side of a signal line 2. Although this modification has a same visual effect as the display panel explained with reference to FIGS. 4 and 5, it has a slight difficulty in the manufacturing process. A source wiring of the TFT 3 requires a crossing a with a drain wiring of the TFT 3'. Therefore, a multiple wiring technique is required in the manufacturing process in addition to the photolithographic technique and etching technique which are mainly required in the production of the display panel shown in FIGS. 4 and 5.

Another modification is shown in FIG. 7 in which TFT's 3 and 3' are disposed on both sides of the scanning line 1. This modification does not require the multiple wiring technique, unlike the modification shown in FIG. 6. However, because the scanning line 1 cannot be directly used as gates of both TFT's 3 and 3', additional conductive layers continuous to the scanning line 1 are required for the gates of the TFT's 3 and 3'. These additional conductive layers occupy only a small additional area for the driving circuit on the display panel and do not require a particular production technique with a mask change for etching. Therefore, this modification provides almost the same advantages in the visual effect and the production technique.

The second embodiment of the present invention has four sets of TFT's and liquid crystal display elements for one picture element as shown in FIGS. 8 and 9. The arrangement of one picture element is shown in FIG. 8. Two TFT's 3 and 3''' are disposed on the right-hand side of the signal line 2 and the remaining two TFT's 3' and 3'' are on the left-hand side thereof. Two TFT's 3

and 3' are on the lower side of the scanning line 1 and the remaining two TFT's 3" and 3"' are on the upper side thereof. All the gates of the four TFT's are connected to the scanning line 1. All the sources are connected to the signal line 2. The drains of the TFT's 3, 3', 3" and 3"' are respectively connected to lower electrodes of the four liquid crystal display elements to drive liquid crystals 5, 5', 5" and 5"' which are respectively disposed between the lower electrodes and a common upper electrode 6.

The driving circuit panel is shown in FIG. 9, a plurality of scanning lines 1 and a plurality of signal lines 2 are disposed on a glass substrate 10. At every crossing point, four TFT's and four lower electrodes are disposed to form one picture element. The lower electrodes 4, 4', 4" and 4"' are made of a transparent conducting layer of Indium Tin Oxide (ITO), each size being 100 $\mu m \times 100$ μm. The whole surface is covered with liquid crystal such as the twisted nematic type via a shading layer, a passivation film and an orientation film. A cover cap having a transparent conductive film on the inner surface as the common electrode 6 is disposed on the liquid crystal.

The manufacturing process of this driving circuit panel does not require the multiple wiring techniques, similar to the first embodiment shown in FIGS. 4 and 5. It can be constructed with a standard LSI production technique skilled in the art. As explained in the first embodiment, the production yield is assumed as 99.9%. The display panel is assumed to have a matrix of picture elements of 500 rows and 500 columns. The number of necessary TFT's is 1,000,000. Among them, defective TFT's are 1,000, causing 1,000 non-working liquid crystal display elements. The number of half-defective picture elements, that is, the picture elements in which two TFT's are defective, is 1. The number of ¾ defective picture elements in which three TFT's are defective is 1/1000, that is, one panel among 1,000 panels. The number of completely defective picture element in which four TFT's are all defective is only 1/1,000,000. Thus, according to the second embodiment, the possibility that one picture element is completely defective is negligible. If a part of one picture element is defective, the remaining effective part of the picture element presents information of the picture element with a reduced area. Therefore, even if defective TFT's are involved in the display panel of the second embodiment, they do not affect the visual image on the display panel. Such effect is similarly obtained if the production yield of TFT's is lowered to 99%. The imperfectness of the image on the display panel may be perfectly compensated by driving liquid crystal in the effective parts of the picture elements to make the transmittance 4/3 times when three TFT's are effective in one picture element, two times when two TFT's are effective and four times when one TFT is effective. The control of the transmittance may be achieved by voltage at the signal line which is raised in synchronism with the drive of the set of TFT's including defective TFT or TFT's by using semiconductor memories.

Although some preferable embodiments are explained above, it is apparent for those skilled in the art that the present invention can be successfully applied to other types of liquid crystal display panels and that the above explained embodiment can be variously modified. The twisted nematic type of liquid crystal may be changed with other types of liquid crystal. The thin film MOS field effect transistor as a switching element may be replaced by other thin film active elements such as a junction type thin film field effect transistor, a thin film bipolar transistor or a thin film diode.

What is claimed is:

1. A liquid crystal display panel comprising:
a plurality of scanning lines arranged in parallel and each receiving a scanning signal;
a plurality of signal lines arranged in parallel and crossing said scanning lines perpendicularly to form a matrix of crossing points, each of said signal lines receiving a driving signal;
a plurality of switching elements disposed at said crossing points such that at least a pair of switching elements are disposed at every crossing point and simultaneously switched by the same scanning and signal lines at each of said crossing points; and
a plurality of liquid crystal display elements coupled with said switching elements, each one of said liquid crystal display elements being associated with one of said switching elements, and said plurality of swtiching elements, when all are non-defective, driving simultaneously all the associated liquid crystal display elements with each driving signal.

2. A liquid crystal display panel as claimed in claim 1, wherein said switching elements are thin film transistors having a control electrode connected to said scanning line, a common electrode connected to said signal line and an output electrode connected to an electrode of the liquid crystal display element.

3. A liquid crystal display panel as claimed in claim 2, wherein the numbers of said transistors and said liquid crystal display elements at each of said crossing points are respectively two.

4. A liquid crystal display panel as claimed in claim 2, wherein the numbers of said transistors and said liquid crystal display elements at each of said crossing points are respectively four.

5. A liquid crystal display panel as claimed in claim 2, wherein said thin film transistors are MOS field efect transistors having a gate connected to said scanning line, a source connected to said signal line and a drain connected to the liquid crystal display element.

6. A liquid crystal display panel as claimed in claim 5, wherein the number of said MOS field effect transistors at each of said crossing points is two.

7. A liquid crystal display panel as claimed in claim 5, wherein the number of said MOS field effect transistors at each of said crossing point is four.

8. A driving circuit of a liquid crystal display panel comprising:
a substrate having an insulative surface;
a plurality of scanning lines disposed on said substrate;
a plurality of signal lines disposed on said substrate and crossing said scanning lines orthogonally forming a matrix of crossing points;
a plurality of sets of four thin film transistors, one of said sets being disposed adjacent each crossing point of said scanning lines and said signal lines such that each of said thin film transistors are arranged on every quartered plane defined by said scanning and signal lines, each set of said four thin film transistors having control electrodes commonly connected to one of said scanning lines, electrodes commonly connected to one of said signal lines and output electrodes such that each

transistor in said set of four thin film transistors is driven by the same scanning and signal lines; and

a plurality of electrode pads connected to said output electrodes of said thin film transistors, respectively, to apply driving voltages to liquid crystal through said thin film transistors in response to signals at said scanning and signal lines.

9. A driving circuit of a liquid crystal display panel comprising:

a substrate having an insulative surface;

a plurality of scanning lines disposed on said substrate in parallel;

a plurality of signal lines disposed on said substrate in parallel, said signal lines perpendicularly crossing said scanning lines to form a matrix of crossing points;

a plurality of pairs of thin film transistors, two of said pairs being disposed adjacent each one of said crossing points, one of said pair of thin film transistors being on one side of each of said signal lines, the other of said pair of thin film transistors being on the other side of each of said signal lines, and each of said pairs of thin film transistors having control electrodes connected to the same scanning lines at each of said crossing points, common electrodes connected to the same signal lines at each of said crossing points and output electrodes; and

electrode pads respectively connected to said output electrodes of said thin film transistors, said electrode pads applying driving voltages to liquid crystal through said thin film transistors in response to signals at said scanning and signal lines.

10. A driving circuit of a liquid crystal display panel comprising;

a substrate having an insulative surface;

a plurality of scanning lines disposed on said substrate in parallel;

a plurality of signal lines disposed on said substrate in parallel, said signal lines perpendicularly crossing said scanning lines to form a matrix of crossing points;

a plurality of pairs of thin film transistors, one of said pairs being disposed adjacent each one of said crossing points, one of said pairs of thin film transistors being on one side of each of said scanning linses, the other of said pairs of thin film transistors being on the other side of each of said scanning lines, and each of said pairs of thin film transistors having control electrodes connected to the same scanning lines at each of said crossing points, common electrodes connected to the same signal lines at each of said crossing points and output electrodes; and

electrode pads respectively connected to said output electrodes of said thin film transistors, said electrode pads applying driving voltages to liquid crystal through said thin film transistors in response to signals at said scanning and signal lines.

* * * * *